Abstract of the Disclosure

When threshold voltages of constituent transistors are reduced in order to operate an SRAM circuit at a low voltage, there is a problem in that a leakage current of the transistors is increased and, as a result, electric power consumption when the SRAM circuit is not operated while storing data is increased. Therefore, there is provided a technique for reducing the leakage current of MOS transistors in SRAM memory cells MC by controlling a potential of a source line ssl of the driver MOS transistors in the memory cells.